ADC-HVC issues with ARGOS BCU

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TABLE OF CONTENTS

1 Change Record

Issue	Date	Section/ Paragraph Affected	Reasons / Remarks	Name
1.0	14.03.2013	all	created	Busoni

2 Scope

This reports describes the tests done to clarify the issue of piezo head oscillations arisen during Arcetri tests in March 2013 with the new BCU with ADC board.

4 Introduction

After the installation of the new BCU with the ADC board, we are no more capable of operating the piezo mirrors together with the frame grabber. When the frame grabber is configured the piezo mirrors start to oscillate and produce an horrible sound.

5 Definitions

We refer to the BCU ADC board as “ADC board”.
We refer to the BCU High Voltage Controller board as “HVC board”
We refer to the PI S334 piezo tip-tilt head as “piezo head”
We refer to the 2nd piezo port of the 2nd HVC board (I/O 3,4 and 5) as “channel 3”.
We refer to the Quantum delay generator that sends a trigger signal to the pnCCD electronics as “delay generator”.
We refer to the pnCCD sequencer board sending triggers to the ADC board as “sequencer”.
We refer to the noise produced by the piezo head oscillation as “the Noise”.

6 Test Conditions

The Pockels cells High Voltage Controller is off (to avoid electromagnetic noise).
The delay generator generates a trigger every 10ms to the pnCCD sequencer.
A piezo head is connected to the channel 3. The tests have been done also using the other ports, giving the same result.
An oscilloscope is connected with to sniff channel X and Y of the piezo head.
A monitoring sw tool is reading data from the HVC during operation and storing on disk for off-line plotting. Typical acquisition rate is around 70Hz. Most of the variables of the HVC local actuator servo control loop are accessible.
The master diagnostic downloaded from the BCU (when configured) is analysed to extract slopes and HVC commands and is dumped on file.

7 Facts

1. When the Noise is present the following conditions are always met (these conditions are necessary but not sufficient) :
   I. The DSP code in the ADC board has been started
   II. The DSP code in the HVC board has been started
   III. The HVC relais are enabled.
2. The noise frequency scales with the frequency of the delay generator. Always.
3. Each of the 3 mirrors produces noise.
4. The noise is audible with mirror rested and with mirror set. The volume is bigger when the mirror is set.
5. There is no audible difference when piezos are operated in closed loop or in open loop.

6. When the noise is not audible all the diagnostics under our control indicate that the mirror is performing correctly as it was during our test of some months ago.

8 Test description

8.1 No-frames rested case.

This test is to show the noise sensitivity of the tools.

The BCU is reset (red button)
The HVC board is configured. See detailed description below.

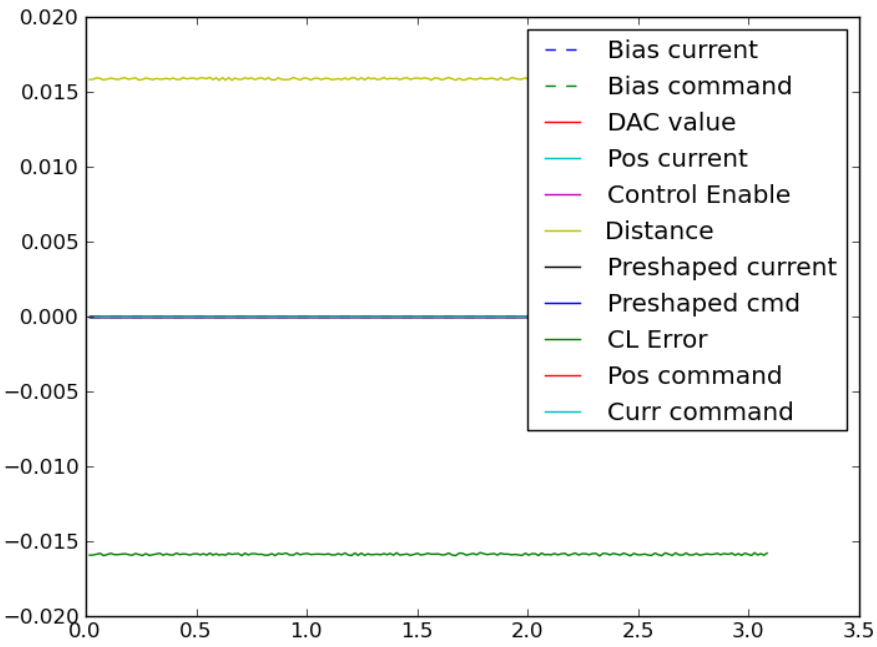

Figure 1 Monitor tool plot shows data collected for piezo x-axis. On abscissa is time in seconds. Values shown are control loop variables in radians. "Distance" is the strain gauge value, i.e. the actual angle value (converted in radians, according to the piezo head calibration). Angular range is 0-30 mrad. In this example, the mirror is rested (close to its central value 15mrad) and all the mirror commands are still to be set. The angle measurement is affected by a small error ("distance" rms << 1mrad)

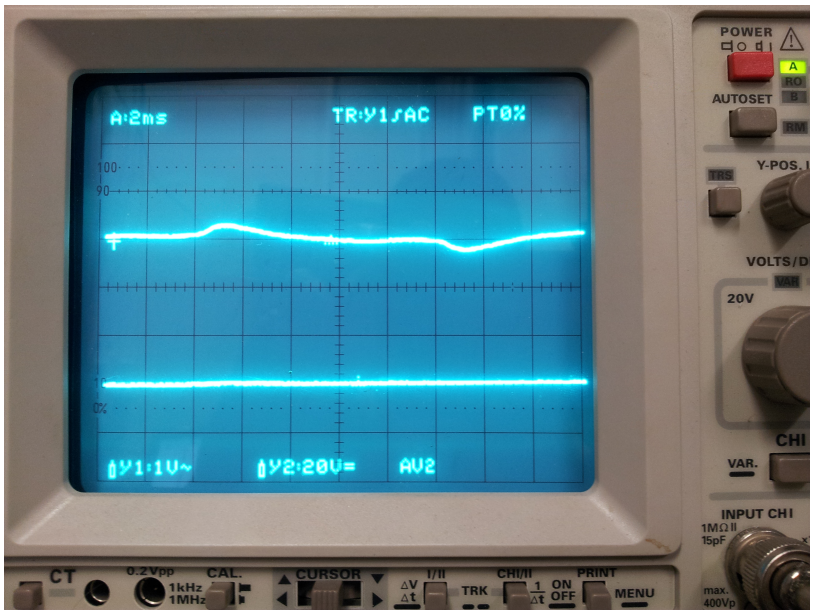

Figure 2 Oscilloscope has been set to show AC values on channel 1 (corresponding to piezo X axis) and DC values on channel 2 (piezo Y axis). A 500mV oscillation at 50Hz is visible.

8.2 No-frames set Ready case.

This is the standard piezo setReady operation, with no frame-grabber configuration. The mirror goes to the nominal position without any problem. No oscillations are visible. The Noise is not audible.

The BCU is reset (red button)
The HVC board is configured. See detailed description below.
The Channel 3 is set to nominal position. See detailed description below (setReady).

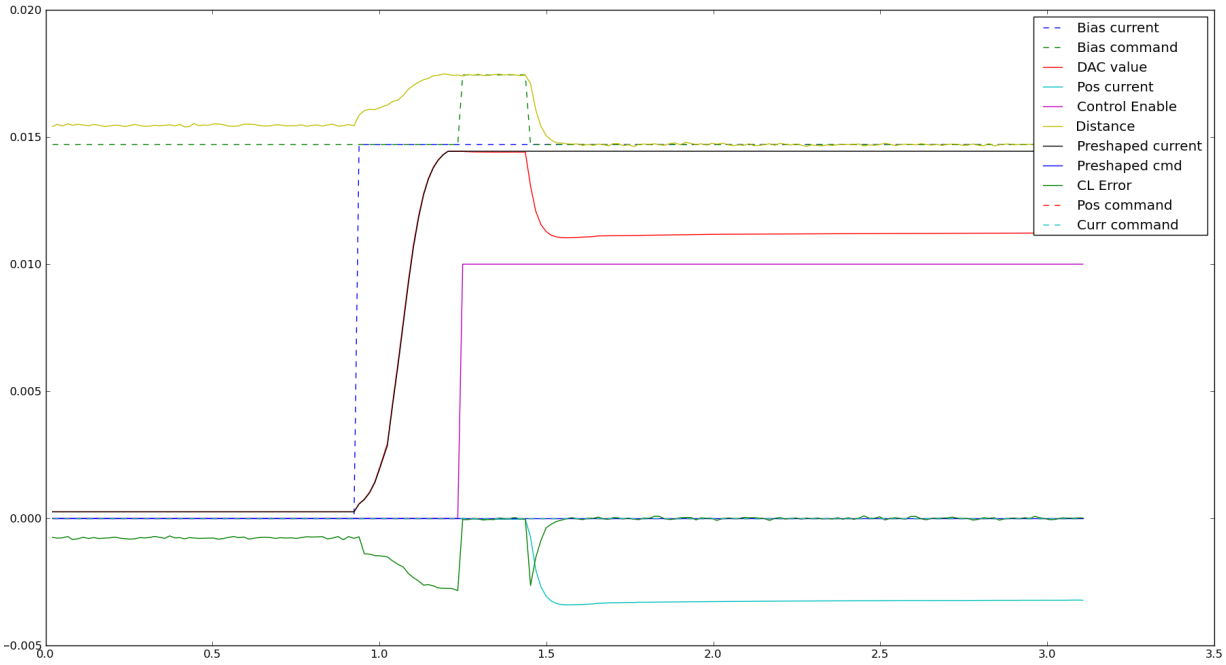

Figure 3 monitor of setReady. Mirror is set to nominal position and control loop is closed (magenta signal). Control loop error (green) goes to 0, DAC value (input to the piezo HV amplifier) is set to reach the desired position. The "distance" error is still small.

8.3 Frames and setReady case. The Noise appear.

When the frame grabbing is enabled the Noise appear.

The BCU is reset (red button)
The HVC board is configured. See detailed description below.
The Channel 3 is set to nominal position. See detailed description below (setReady).
The ADC board is configured (standard)
The Sequencer is started.
The Noise is audible.

The masterdiagnostic (dump is in diagnostic_0weights_noise_setready.txt) confirms that slopes are all 0 and HVC mean voltage are 0. So the TT compensation algorithm is not actuating the piezo mirror and the Noise is due to something else.

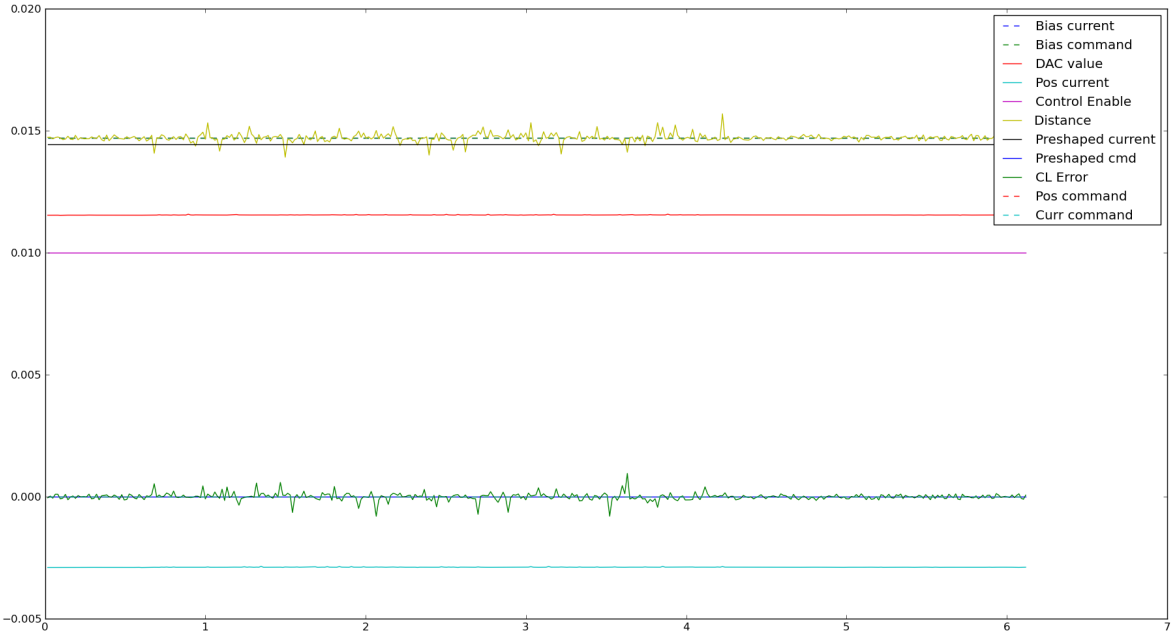

Figure 4 At time 0.5 the Sequencer is started and the piezo mirror start to oscillate and emits the Noise. At time 4s the sequencer is stopped

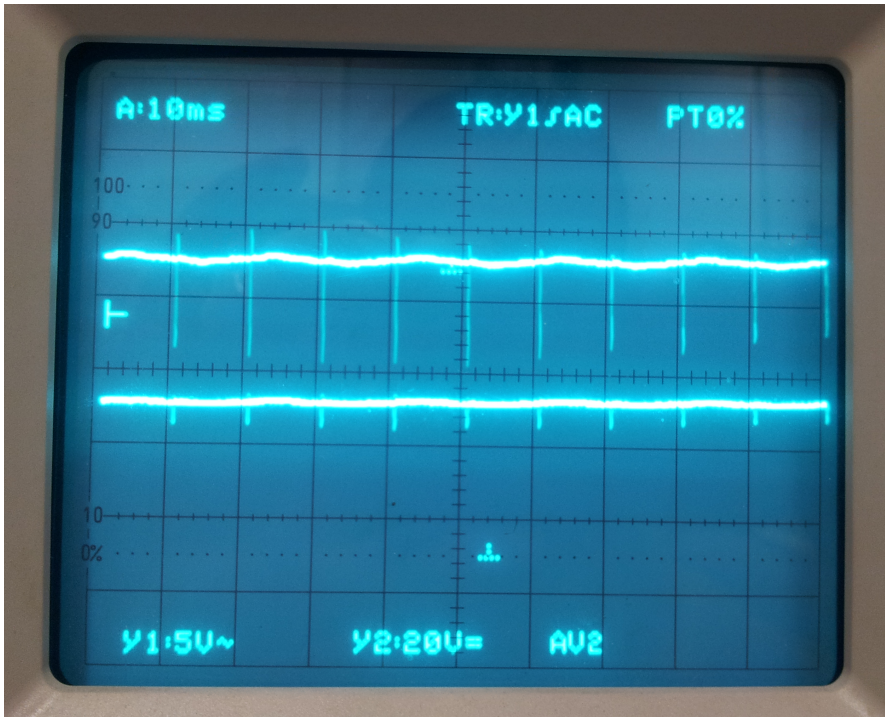

Figure 5 When the Noise is present the actuators signals show a disturbance at 100Hz (same frequency of the Trigger) of 10V amplitude.

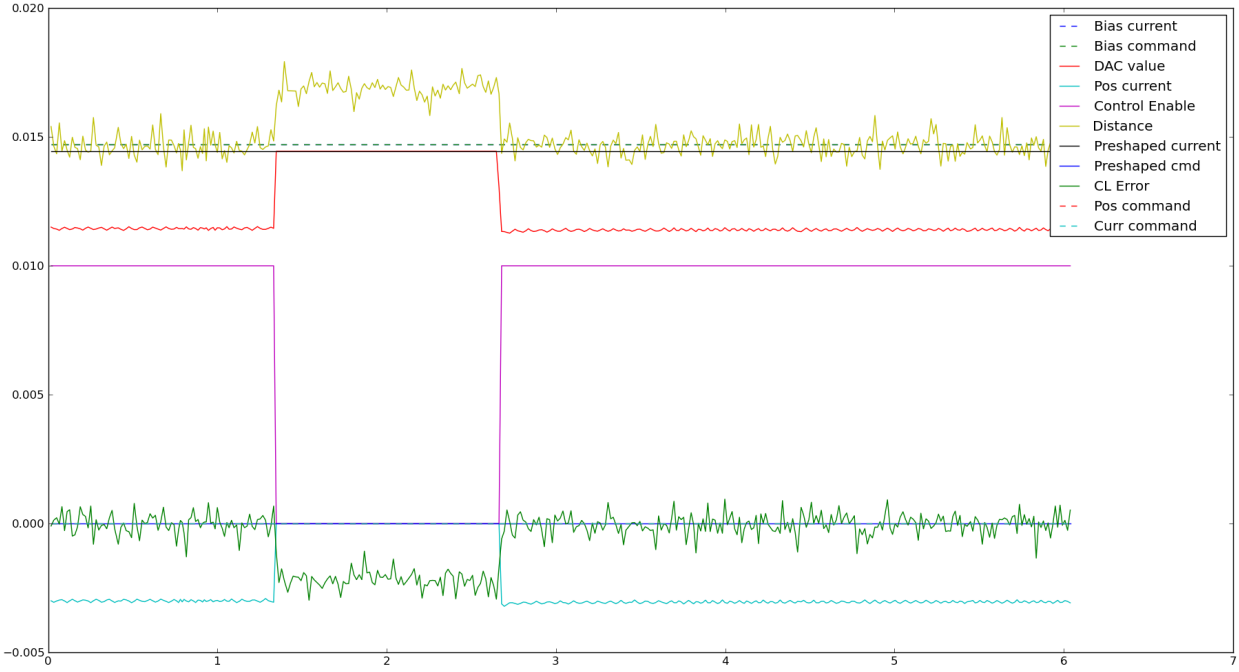

Figure 6 We put the piezo mirror in open-loop (from 1.5 to 2.5s). The HVC DAC is not actuated (constant value) still the Noise is there as evident from the "distance" rms. It is not an effect of the closed-loop.

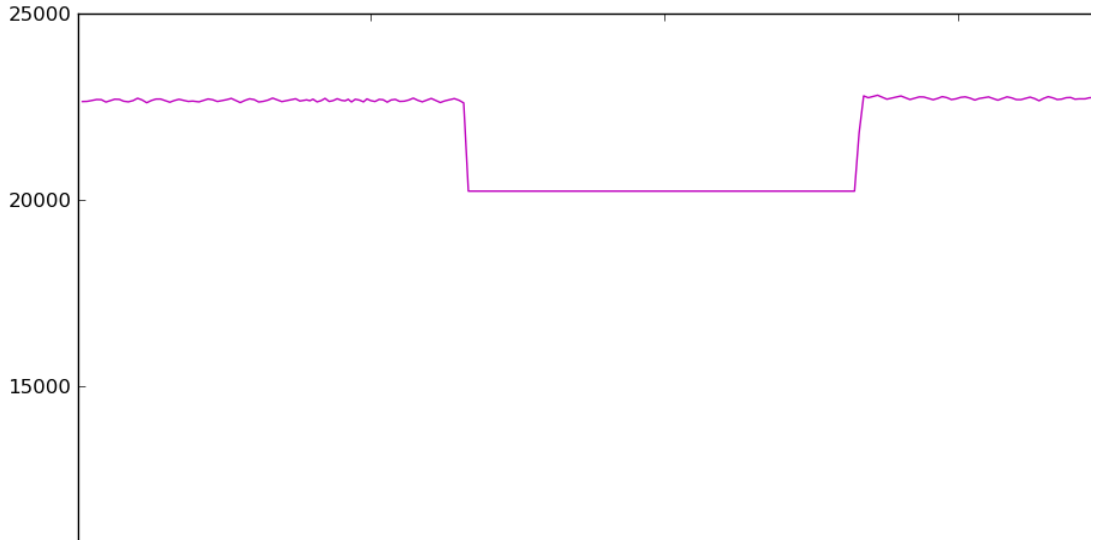

Figure 7 HVC uint_DAC_value is also constant when in open-loop.

8.4 Other tests

We did some additional test to identify a minimal configuration that conduce to the Noise.

1. ADC configuration
2. Start Sequencer
3. HVC minimal start (see below)
4. HVC enable relais
5. **The Noise appears.**

1. ADC configuration
2. Start Sequencer
3. HVC enable relais
4. HVC minimal start (see below)
5. **The Noise appears.**

1. HVC enableRelais
2. HVC minimal start (see below)
3. Configure ADC board without enabling ADCs (ADCBoardSelection=0)
4. Start Sequencer
5. **No Noise**

1. HVC enableRelais
2. HVC minimal start (see below)
3. Configure ADC board with ADC (ADCBoardSelection=1)
4. Start Sequencer
5. **The Noise appears**

(this proves that the BCU board is not related to the problem)

1. Stop the Sequencer
2. HVC full configuration
3. HVC enableRelais
4. ADC board minimal start (see below)

The Noise appears even if the Sequencer is disabled and frames are not grabbed.

The Noise is a little bit different (100Hz with some <1Hz modulation). If the trigger cable between Sequencer and BCU is unplugged the Noise disappear. If the cable is re-plugged, the Noise is back. Somehow the clock signals in the Sequencer cable are enough to generate the Noise.

9 Detailed description of BCU configuration

9.1 HVC configuration

1. The DSP code in the 2 HVC boards is uploaded.
2. The DSP memory is configured, using the calibrations measured for the piezo-head.
3. The HVC DSP code is started and ISR is enabled.
4. Output relais are disabled.

This configuration has been used in the past months and is proved to be effective and safe for the piezo heads. It has been tested with the previous version of the BCU, without any frame-grabbing capability.
The SelectionMatrix, CommandOffset, RotationMatrix are set to zero to prevent the TTCommandVector to be applied as input to the HVC code.

9.2 HVC Minimal configuration

1. Upload DSP code
2. Start DSP code
3. Enable ISR

9.3 HVC channel: setReady

HVC is configured (see above).

1. Preshapers are set to 0.2s.
2. Output relais are enabled.
3. Commands (pos_command and curr_command) are set to 0.
4. Bias_current is set to mid-range (approx. 15mrad)
5. Wait 0.3s
6. Distance is read and bias_command is set to the actual distance
7. Control loop is enabled.
8. Wait 0.2s
9. Bias_command is reset to mid-range (approx. 15mrad)
10. Preshapers are reset to the original value (5-10ms)

9.4 ADC board configuration

The ADC board is configured for frame acquisition and slope computation. Master diagnostic is enabled. Weights in the subaperture definitions are put to 0 to obtain null slopes. The actual computed slopes are checked on the master diagnostic streams, and are confirmed to be null.

1. argos_bcu_configure_adc_slope_computation.py
2. argos_bcu_gox_slope_configuration.py [weights=0]
3. argos_bcu_enable_master_diagnostic.py

A similar configuration using Alfio's configuration routines give the same results.

9.5 ADC board minimal configuration

1. Upload DSP code
2. Write 0 in TS201_START_ADDR
3. Set ADCBoardSelection to 1

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