GIANO

The Versatile Acquisition System of Giano

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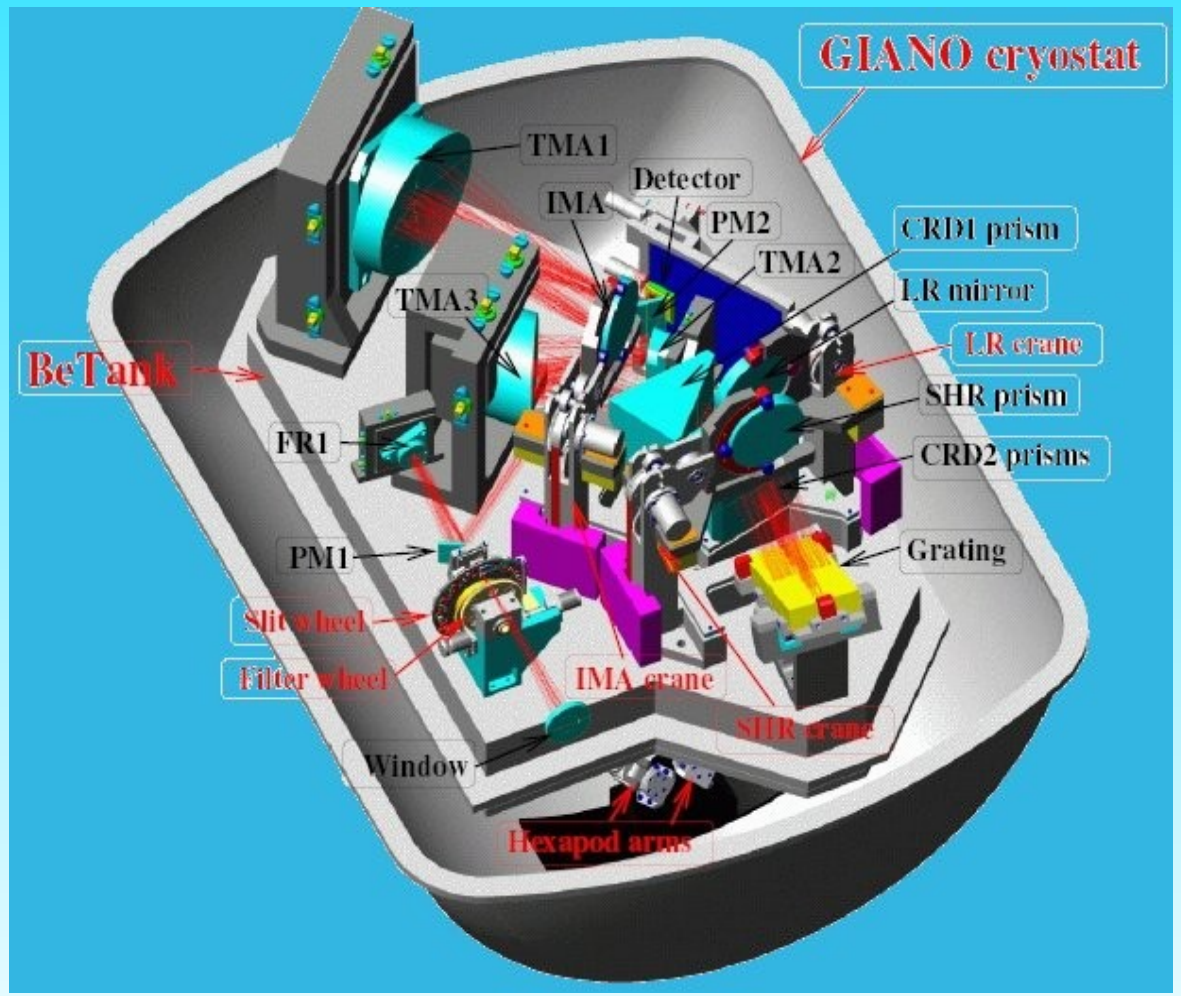
INAF-OAA, INAF-OABO, INAF-CGG, INAF-IRA

Giano spectrometer

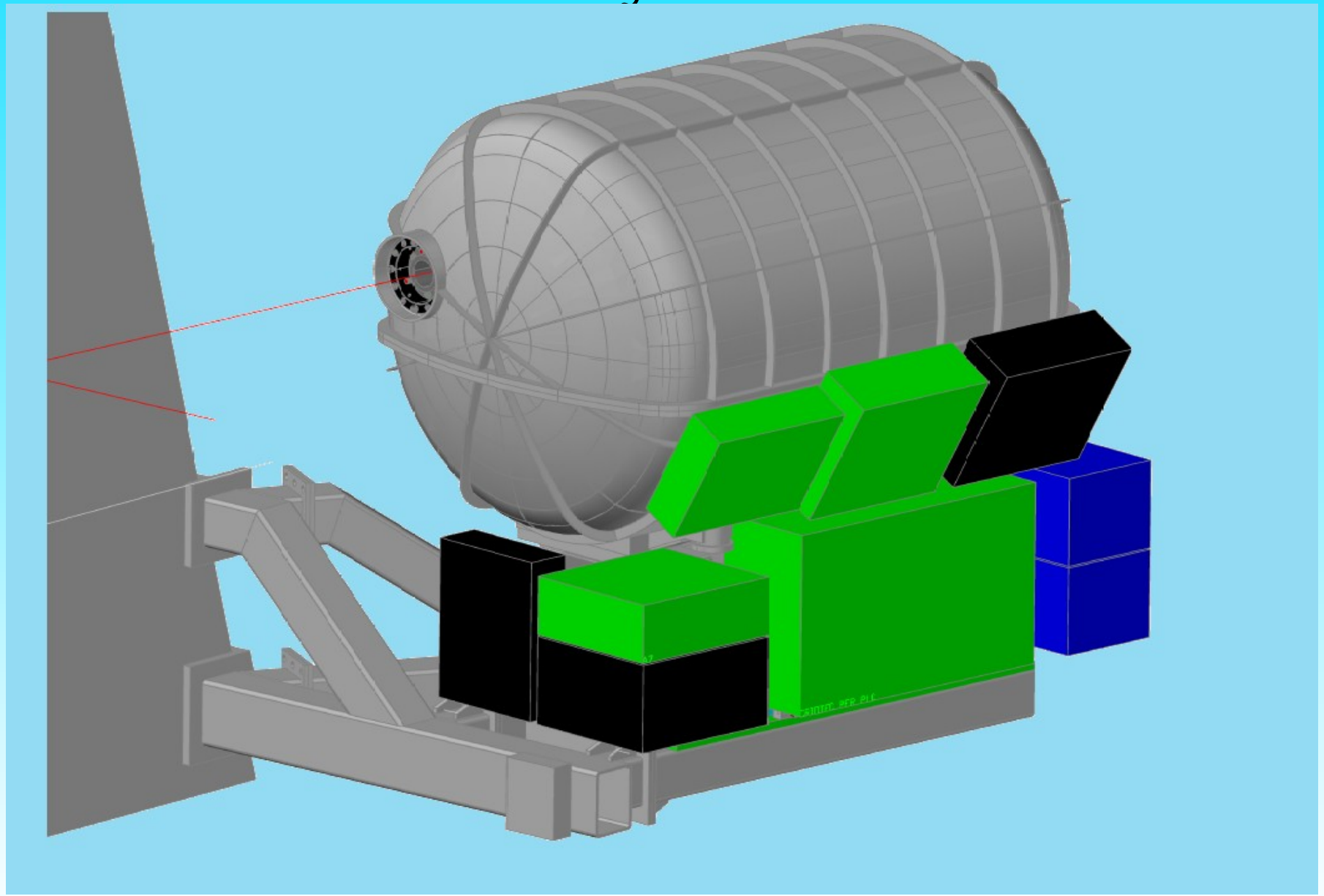


To be installed at

The TNG
The Galileo Italian
National Telescope
La Palma

GIANO

At Nasmyth B of TNG

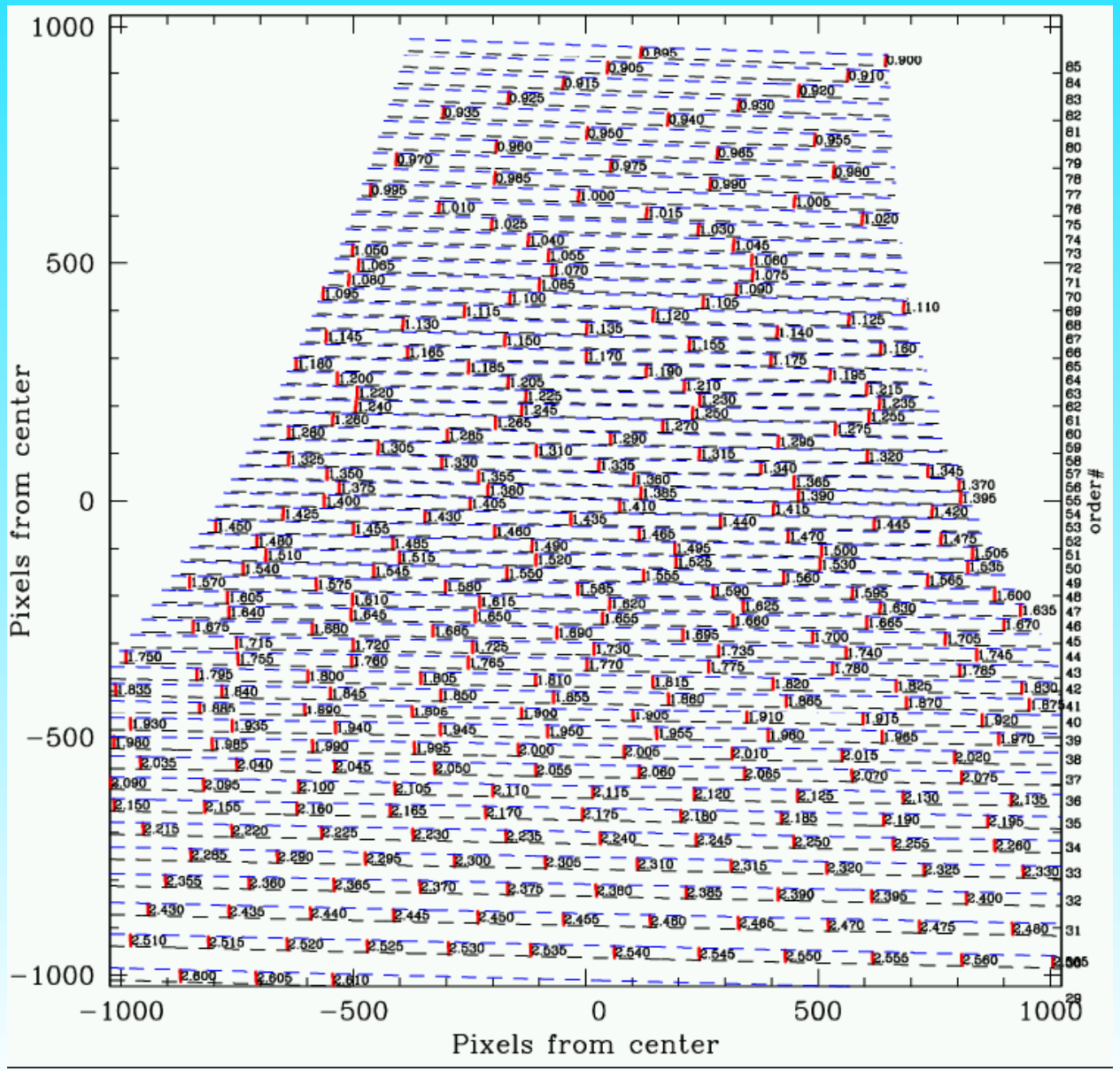


Main characteristics

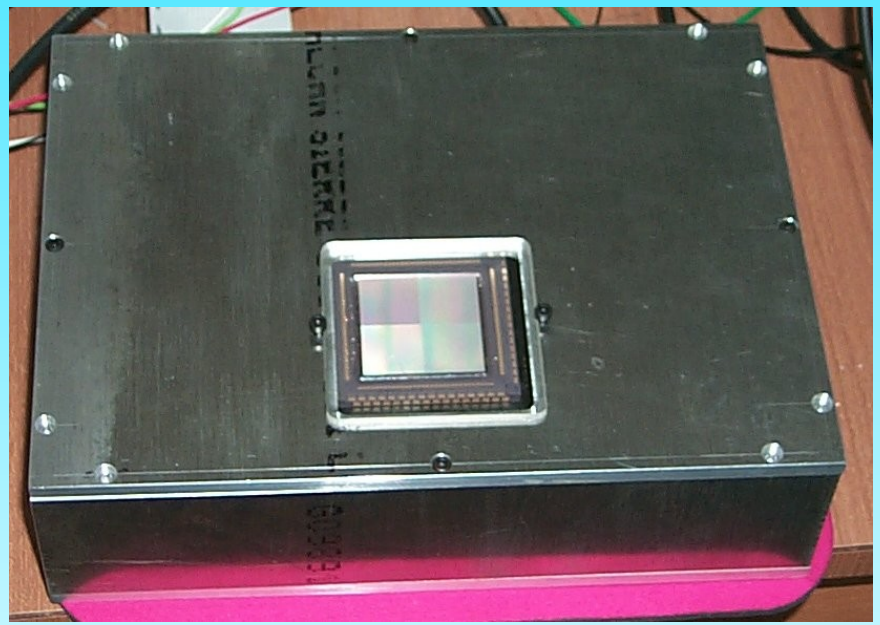
- All Near-IR spectrum measured in a single shot
- High Resolution up to R=46,000 Range=0.9-2.5μm
- Low Resolution R=400 Range=0.9-2.5μm
- Common users instrument: always at telescope

Echelle Spectrograph

Near total coverage of 0.9-2.6 μm wavelength range.



Giano Detector



- **2K x 2K Hawaii2**
- 18 μm Pixel Pitch
- 0.7-2.5 mm range
- Multiple Modes
- Low Dark Current (<1 e^-/sec)
- Low Read Noise (<10 e^-)
- Q.E. > 60%
- 3-6 mV/e^-
- Well Capacity ~ 10^5 e^-
- Low Glowing

The acquisition system development guidelines

- The system is divided in several *modules* with clear boundaries.
- We use, as far as possible, commercial parts at board level.
- We use largely accepted standards as boundaries, as a PCI bus, an industrial standard PC104 bus or an Ethernet connection.
- We designed the custom parts as concepts, not around a particular electronic device.
- The waveform generation is as flexible as possible
- Design from Fasti, reusing as much as possible.

General Structure

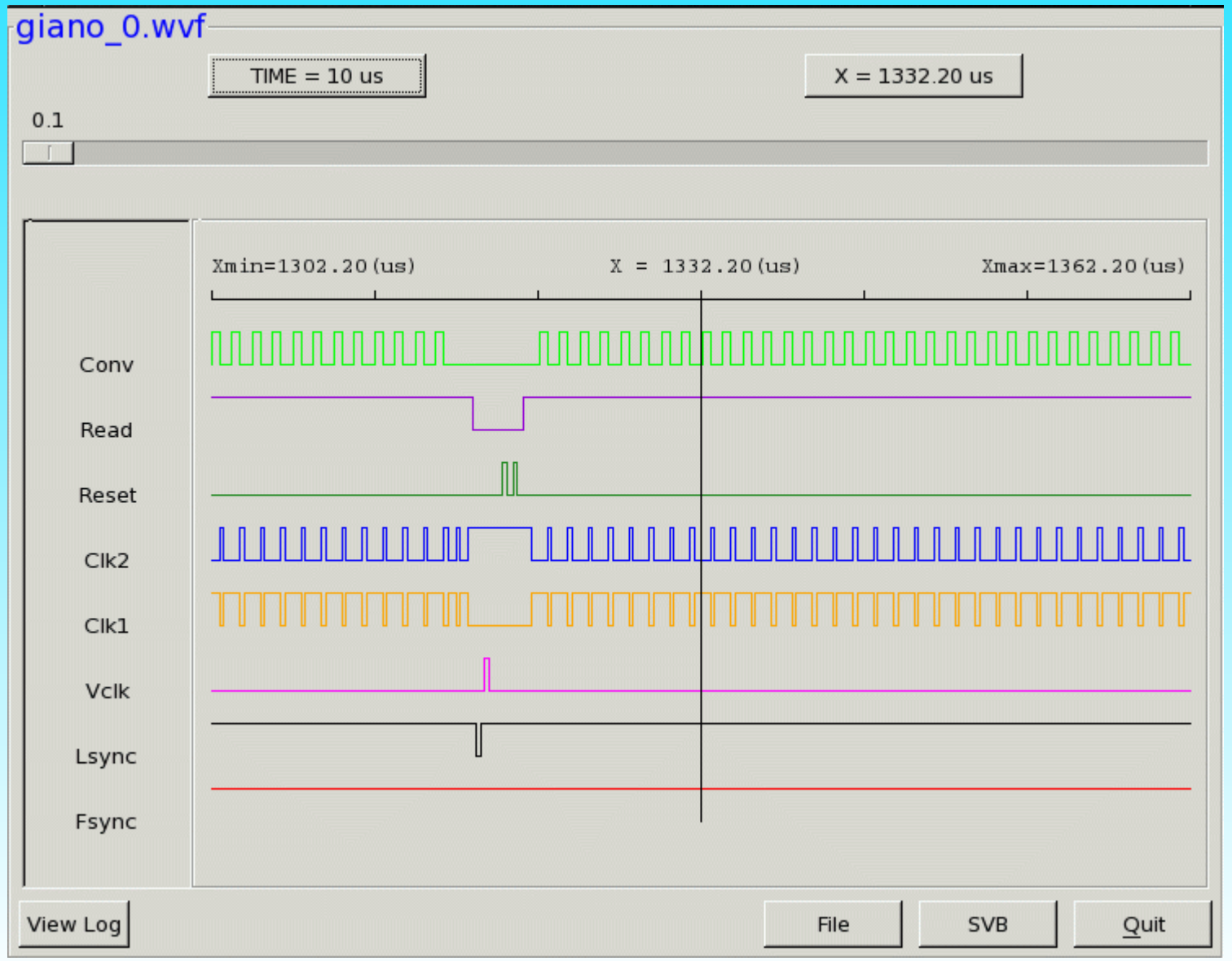
- Detector board and preamplifier
- Bias and clock generation, conversion
- Data buffers, PC104 interface
- An embedded system as general controller
- The main data collection PC
- The user interface PC

Clock Generation

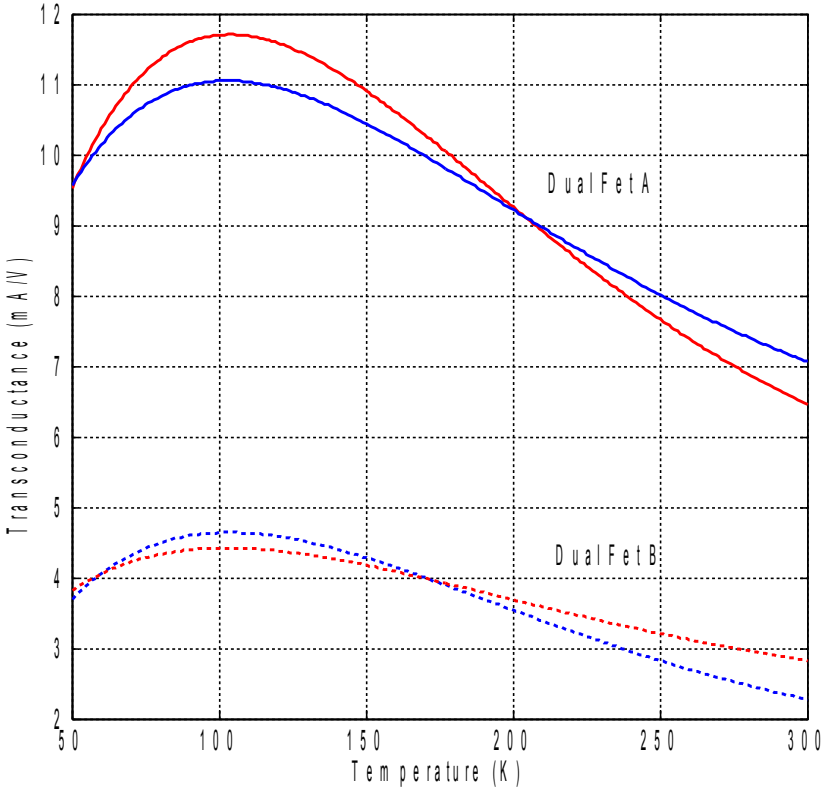
Two different approaches:

- Custom micro-controller based (patented), with specialized micro-assembler. It is implemented in a Altera FPGA. Software available: assembler, emulator, visualizer. Very flexible, precious in laboratory, steep learning curve.
- Programmable sequence of *waveform macros*. Also implemented in Altera FPGA, small and fast. Easy to use, but lack the 'what if' flexibility. To be used at telescope.

Sequence emulator display



Preamplifier



- Cold preamplifier.
- Discrete components based (U440 Dual-FET)
- Selection of FETs
- Noise proportional to $\sqrt{T/G_m}$
- Noise better than $2\,\mathrm{nV\,Hz^{-1/2}}$
- Better read-out noise
- Better cross-talk immunity

Cfr. Biliotti et al. Submitted to AJ, 2006

The acquisition chain hardware

- The conversion board
- The buffer board
- The embedded system

The conversion boards

- 4 or more boards: one on each detector output
- Fast 18 bit AD7674, used at 500KS/Sec
- Faster 16bit+average option (up to 4MS/Sec)
- Fault-tolerant design
- Control logic on a Altera FPGA
- FlexConnect© to detector cold board
- Copper or fiber optics LVDS up link
- Hosts also the biases generation

The buffer board

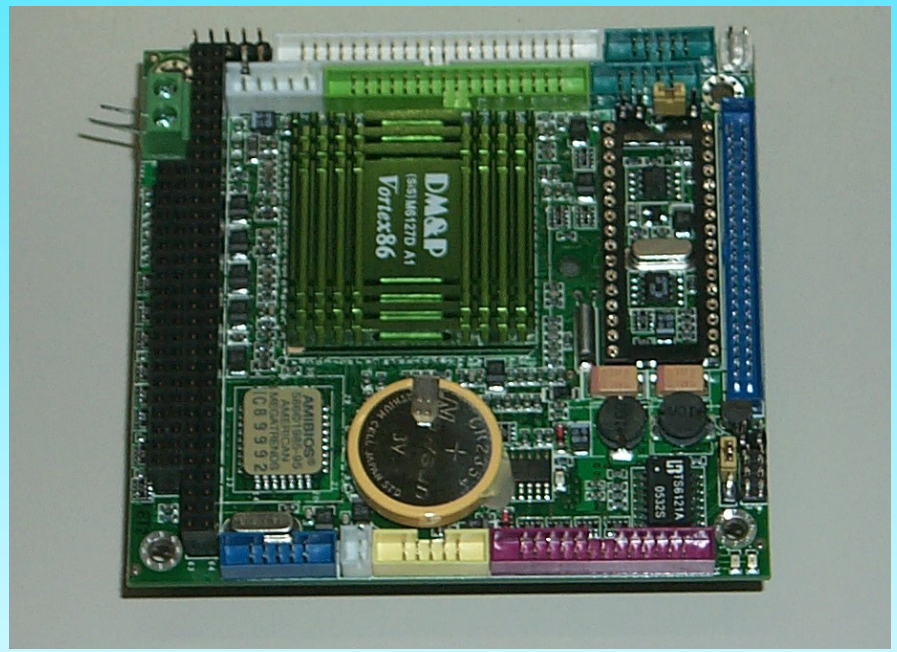
- Control logic based on a FPGA
- 2 full frame memory capacity
- Up to 32 LVDS input capabilities
- Link to a PC104 or a PCI bus
- Fifo mode operation
- Movable memory window mode

The embedded System

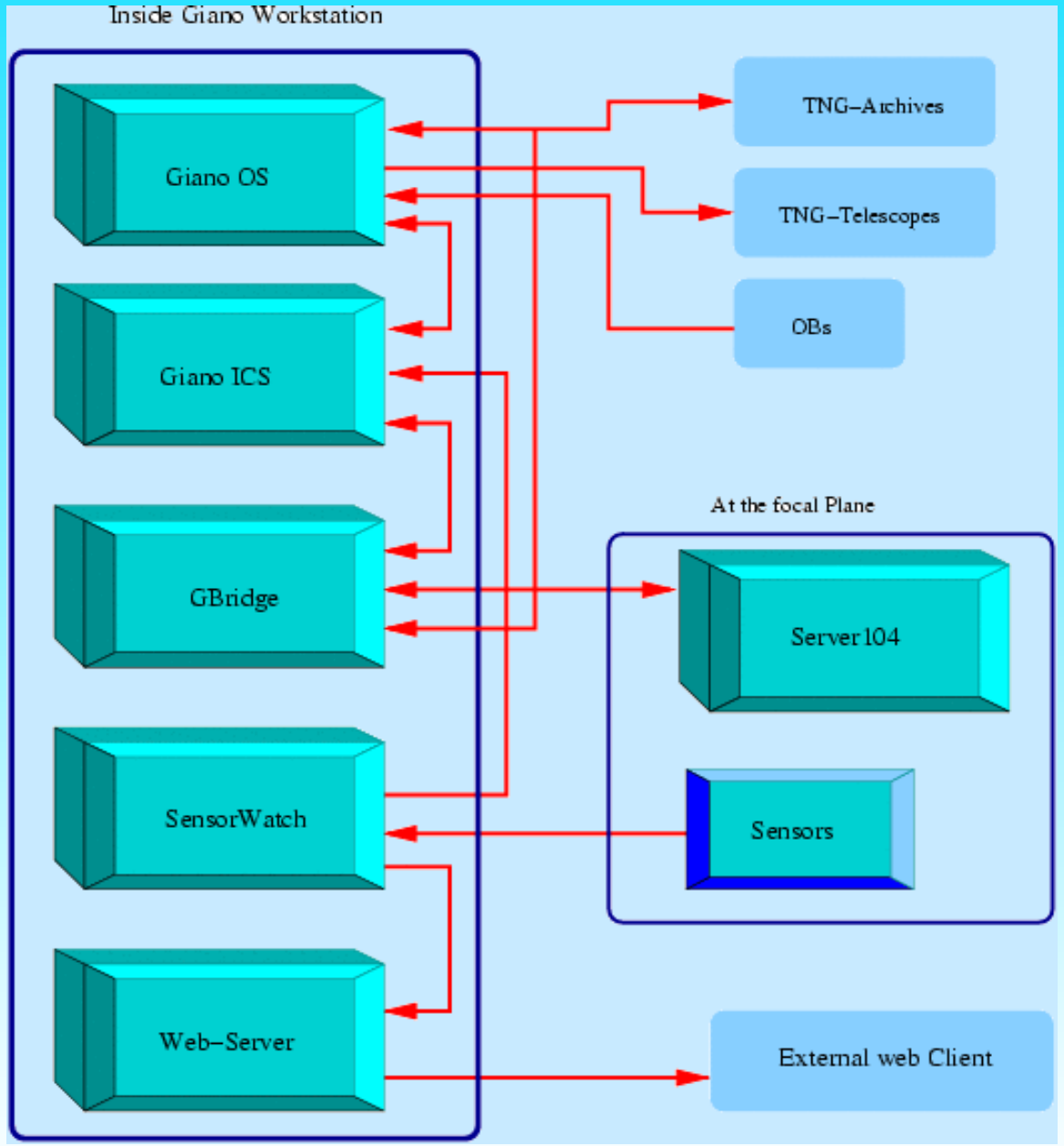
- An industrial standard single board computer
- The actual device is a x86 based PC104 board
- Connected by means of PC104 bus and Ethernet
- Embedded Linux, Slax server distribution
- Flexible, rich in stable libraries and applications
- Possibility of remote maintenance

The PC104 Board

- x86 based
- Low power (~5W)
- Fanless
- Upgradeable memory
- Smart Card disk



Giano software structure



Low Level Software - I
Server104

- A network daemon inside the embedded system.
- It does all initialization, housekeeping and control for data acquisition.
- It communicates by means of a network socket.
- It programs the waveform generator for the current acquisition mode (correlated double sampling, single reading, multiple non destructive read-out, continuous dummy integrations) and process data.
- It collects and communicates some of the telemetry.

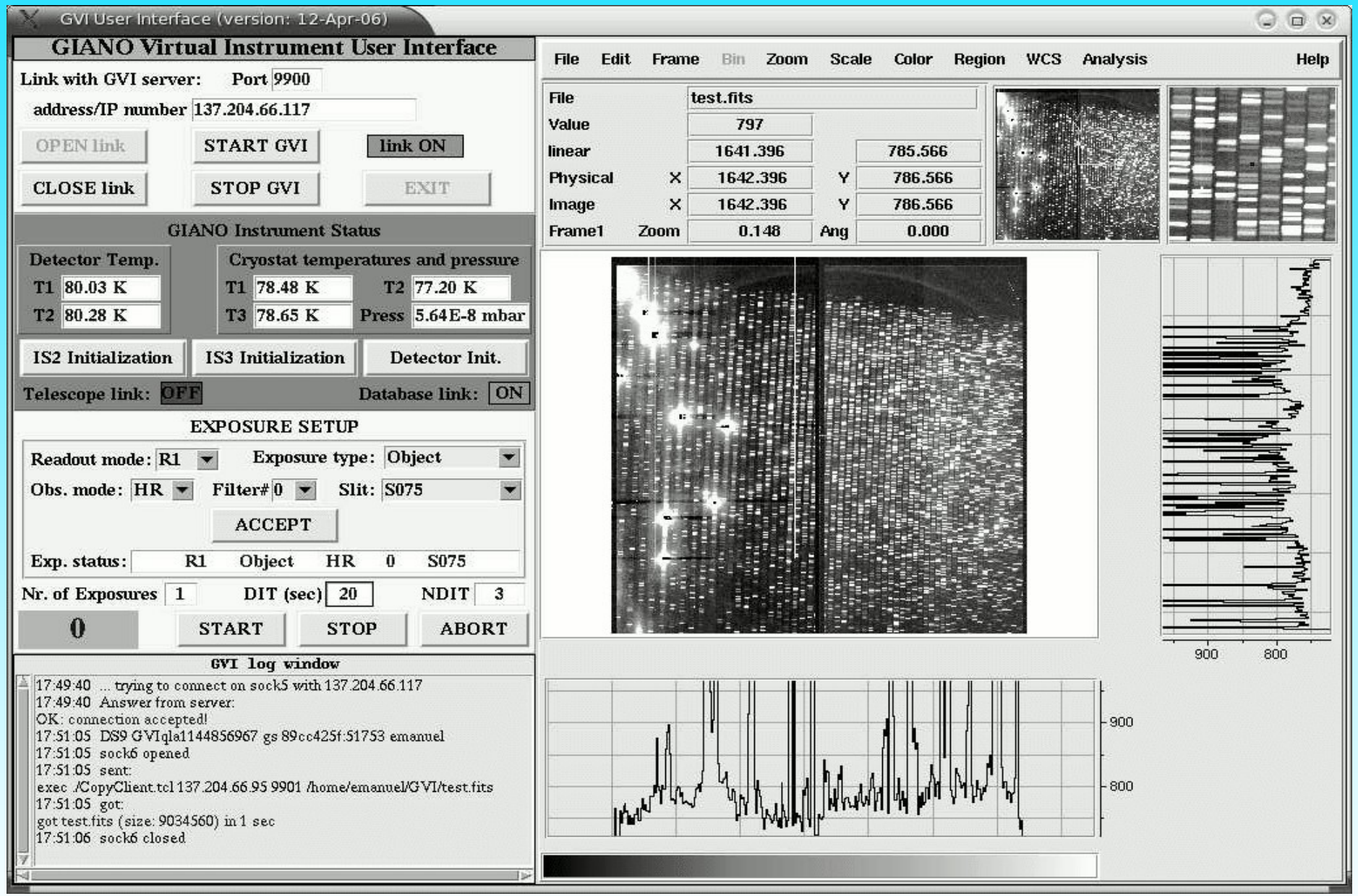
Low Level Software - II
Gbridge

- A middle-ware network daemon in the data acquisition computer.
- It acts as server for User Interface, and as client of Server104.
- It split high level commands in elementary operations, and sends the latter to Server104.
- It controls the integrations, assembles data and archives telemetry in FITS format and sends the resulting files to the archive.
- It has a technical human interface (GuiLab) for laboratory and testing purposes.

The internal communication protocol

- A single protocol format for all Giano internal communications
- All communications in packet form and only one packet format.
- Binary header with destination process ID and checksum.
- ASCII payload on command and messages for ease of debug
- Binary scientific data payload for efficiency.

The Human Interface



More about Giano

- Web general:
  http://stars.bo.astro.it/giano/documents/documents.html

- Web technical:
  http://www.arcetri.astro.it/irlab/doc/gianodoc.php